

CLAIMS

What is claimed is:

- [c1] A method for reducing signed load latency in a microprocessor comprising:
- transferring data from a cache memory to an aligner;
 - generating a sign bit for the data; and
 - transferring the sign bit to the aligner via a bypass.
- [c2] The method of claim 1, further comprising:
- adjusting the data during transfer to the aligner via a data path; and
 - adjusting the sign bit during transfer to the aligner via the bypass.
- [c3] The method of claim 2, further comprising:
- selectively processing a part of the data for use in generating the sign bit.
- [c4] The method of claim 3, further comprising:
- selectively processing the part of the data selected for use in generating the sign bit based on an instruction from a CPU.
- [c5] An apparatus for reducing signed load latency in a microprocessor, comprising:
- a data path connecting a cache memory to an aligner; and
 - a bypass connecting the cache memory to the aligner;
- wherein data is transferred from the cache memory to the aligner via the data path and a sign bit for the data is transferred from the cache memory to the aligner via the bypass.

- [c6] The apparatus of claim 5, further comprising:
a select component for providing a signal to generate the sign bit for the data.
- [c7] The apparatus of claim 5, wherein the bypass comprises:
a sign multiplexer; and
a real-sign multiplexer.
- [c8] The apparatus of claim 6, wherein the select component provides a signal to choose a part of the data and to generate the sign bit for the data based on an instruction from a CPU.
- [c9] The apparatus of claim 5, wherein the aligner comprises a plurality of sub-aligners.
- [c10] An apparatus comprising:
means for transferring data from a cache memory to an aligner;
means for generating a sign bit for the data;
means for transferring the sign bit to the aligner via a bypass;
means for adjusting the data during transfer to the aligner via a data path;
means for adjusting the sign bit during transfer to the aligner via the bypass;
means for selectively processing a part of data for use in generating the sign bit; and

means for selectively processing the part of the data selected for use in generating the sign bit based on an instruction from a CPU.

[c11] An apparatus comprising:

a data path connecting a cache memory to an aligner;
a bypass connecting the cache memory to the aligner;
wherein data is transferred from the cache memory to the aligner along the data path and a sign bit for the data is transferred from the cache memory to the aligner along the bypass;
a select component for providing a signal to generate the sign bit for the data, wherein the select component comprises
a sign mulitplexer; and a real-sign multiplexer, and wherein the select component provides a signal for choosing a part of the data to generate the sign bit for the data based on an instruction from a CPU; and
wherein the aligner comprises a plurality of sub-aligners.